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09/754,406	01/02/2001	Songjie Xu	APLUS.001A	3824

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EXAMINER	
STEVENS, THOMAS H	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/754,406	XU, SONGJIE	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 8/12/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11,13-28 and 32-37 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11,13-28 and 32-37 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claim 1-11,13-28,32-37.

New Examiner

2. Tom Stevens is now presiding in place of Mary Hogan.

Section I: Non-Final Rejection (2nd Office Action)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-11,13-28,32-37 were rejected under 35 U.S.C. 102(b) as being anticipated by Bennett et al., (US. Patent 5,648,913) (hereafter Bennett). Bennett discloses an independent, frequency driven layout system and method for the field programmable gate arrays (abstract).

Claim 1. A method of reducing circuit timing delays, comprising: selecting a first node: sorting fanins (column 15, lines 22-25) of the first node according to slack (positive and negative slack: column 10, lines 40-54) values associated with the corresponding fanins (column 15, lines 22-25), wherein at least a portion of the slack (positive and negative slack: column 10, lines 40-54) values differ in value; and reducing delays (column 4,

lines 40-54) associated with fanins (column 15, lines 22-25) having relatively larger negative slack (positive and negative slack: column 10, lines 40-54) values before reducing delays (column 4, lines 40-54) associated with fanins (column 15, lines 22-25) having relatively smaller negative slack (positive and negative slack: column 10, lines 40-54) values.

Claim 2. The method defined in claim 1, wherein reducing delays (column 4, lines 40-54) is performed recursively.

Claim 3. The method defined in claim 2, wherein recursively reducing delays (column 4, lines 40-54) is performed until the delays cannot be further reduced or timing constraints (column 12, lines 55-67; column 15, lines 18-25) are violated (column 27,lines 58-60).

Claim 4. The method defined in claim 1, wherein selecting the first node comprises: performing a timing analysis (column 10, lines 7-21) on a circuit; determining a delay based at least in part on the timing analysis (column 10, lines 7-21); determining a slack (positive and negative slack: column 10, lines 40-54) value for each critical node of the circuit based on the delay target; and sorting the critical nodes (equates nodes and connections: column 27, lines 48-50) based on the corresponding slack (positive and negative slack: column 10, lines 40-54) values.

Claim 5. The method defined in claim 4, wherein selecting the first node further comprises selecting a critical node having the largest negative slack (positive and negative slack: column 10, lines 40-54).

Claim 6. The method of reducing circuit timing delays, comprising: selecting a first node: identifying critical fanins (column 15, lines 22-25) of first node; and recursively reducing delays (column 4, lines 40-54) associated with at least a portion of the critical fanins (column 15, lines 22-25) of the first node.

Claim 7. The method defined in claim 6, wherein recursively reducing delays (column 4, lines 40-54) is performed on critical fanins (column 15, lines 22-25) having relative larger negative slack (positive and negative slack: column 10, lines 40-54) values before reducing delays (column 4, lines 40-54) associated with fanins (column 15, lines 22-25) having relatively smaller negative slack (positive and negative slack: column 10, lines 40-54) values.

Claim 8. The method defined in claim 6, additionally comprising performing a local transformation on the first node if the reducing delays (column 4, lines 40-54) for at least one of the critical fanins (column 15, lines 22-25) is not successful.

Claim 9. A method of performing circuit delay reduction, comprising: performing a timing analysis (column 10, lines 7-21) on a circuit; determining a delay target based at

least in part on the timing analysis (column 10, lines 7-21); selecting a first output having a negative slack (positive and negative slack: column 10, lines 40-54) based at least in part on the delay target and the amount of first output negative slack (positive and negative slack: column 10, lines 40-54) relative to the slack (positive and negative slack: column 10, lines 40-54) of the other outputs; and performing local transformations on transitive fanins (column 15, lines 22-25) of the first output to improve the negative slack (positive and negative slack: column 10, lines 40-54).

Claim 10. The method defined in claim 9, wherein the first output is a critical output (column 2, lines 60-63).

Claim 11. The method of reducing timing delays for a circuit having primary input nodes (equates nodes and connections: column 27, lines 48-50), at least one primary output node (both primary input and primary output: columns 14 and 15, lines 64-67 and 1-5), and a set of circuit nodes (equates nodes and connections: column 27, lines 48-50) between the PI nodes (equates nodes and connections: column 27, lines 48-50) and the PO nodes (equates nodes and connections: column 27, lines 48-50)(s), the method comprising: a) identifying a first critical path (column 5, lines 35-40) between a first PI node and a first PO node, wherein the first critical path (column 5, lines 35-40) is selected based on ordering the PO nodes (equates nodes and connections: column 27, lines 48-50) by corresponding slack (positive and negative slack: column 10, lines 40-54) values; b) beginning at the least first PO node, attempting to reduce a delay (column

4, lines 40-54) associated with a first circuit node; c) determining if the delay reduction meets a first predetermination criteria (column 4, lines 2-20) (both primary input and primary output: columns 14 and 15, lines 64-67 and 1-5); d) identifying a following circuit node in the critical path (column 5, lines 35-40) if the predetermined critical is not met; e) attempting to reduce a delay associated with the following circuit node; f) repeating c), d) and e) unit the delay cannot be reduced or a set of constraints (columns 16 and 17, lines 45-67 and 1-13, respectively) are violated; g) identifying a second critical path (column 5, lines 35-40) between a second IP node and a second PO node, (both primary input and primary output: columns 14 and 15, lines 64-67 and 1-5; with design choice; repetition) wherein the second critical path (column 5, lines 35-40) is selected based on the ordered PO nodes (equates nodes and connections: column 27, lines 48-50); h) determining an amount of delay reduction still needed for the second critical path (column 5, lines 35-40) after applying the results of the delay reduction for the first critical path (column 5, lines 35-40); and I) beginning at the second PO node, attempting to reduce a delay (column 4, lines 40-54) associated with a second circuit node.

Claim 13. The method defined in claim 11, wherein a critical path (column 5, lines 35-40) is a path that needs to be reduced in delay (column 14, lines 60-63) so as to meet a target constraint (columns 16 and 17, lines 45-67 and 1-13, respectively).

Claim 14. The method defined in claim 11, additionally comprising establishing the criteria (column 4, lines 2-20).

Claim 15. The method defined in claim 11, wherein the method is performed at a logic optimization (column 5, lines 37-39) phase of a circuit design process (column 8, lines 40).

Claim 16. The method defined in claim 11, wherein the method is performed at a mapping phase of a circuit design process (column 8, lines 40).

Claim 17. The method defined in claim 11, wherein the method is performed at a layout phase (column 1,lines 8-22) of a circuit design process.

Claim 18. The method defined in claim 11, wherein the first PI node and the second PI node are the same (stating the output paths define encompass all paths: column 12, lines 28-49).

Claim 19. The method defined in claim 11, wherein the first PO node and the second PI node are the same (stating the output paths define encompass all paths: column 12, lines 28-49).

Claim 20. The method defined in claim 11, wherein a portion of the first critical path (column 5, lines 35-40) overlays a portion of the second critical path (column 5, lines 35-40).

Claim 21. A method of dynamically reducing delays (column 4, lines 40-54) on a critical path (column 5, lines 35-40) of a circuit topology (column 28, lines 3-6), the method comprising: identifying a critical path (column 5, lines 35-40) of the circuit topology (column 28, lines 3-6); selecting a delay target for a primary output associated wit the critical path (column 5, lines 35-40); dynamically reducing a first critical path (column 5, lines 35-40) delay at a first node in closer proximity to a primary input associated with the critical path (column 5, lines 35-40) than to a node in closer proximity of the primary output; storing the reduced delay; and recursively dynamically reducing a second critical path (column 5, lines 35-40) delay beginning at a second node located between the first node and the primary output based at least in part on the stored reduced delay.

Claim 22. The method defined in claim 21, wherein the circuit topology (column 28, lines 3-6) is associated with a standard cell design process.

Claim 23. The method defined in claim 21, wherein the circuit topology (column 28, lines 3-6) is associated with a gate array design process.

Claim 24. The method defined in claim 21, wherein the circuit topology (column 28, lines 3-6) is associated with a programmable logic design process(column 8, lines 40).

Claim 25. A layout-driven logic synthesis design flow, comprising: selecting a desired circuit delay associated with a first output of a circuit path, wherein other outputs are associated with different initial circuit delays; calculating an initial circuit delay associated with the first output; and iteratively reducing the initial circuit delay to achieve the desired circuit delay using a timing optimization (column 5, lines 37-39) process, wherein in an iteration (column 28, lines 6-9), mapping and clustering are used of measure the outcome of the timing optimization (column 5, lines 37-39) procedure, and wherein the timing optimization (column 5, lines 37-39) process uses such measurements to achieve the desired delay, and wherein the result of an interaction of delay reduction is used by a next iteration (column 28, lines 6-9) of delay reduction to determine an amount of delay to reduce.

Claim 26. The method defined in claim 25, wherein the design flow is associated with a standard cell design process (column 8, lines32-34).

Claim 27. The method defined in claim 25, wherein the design flow is associated with a gate array (column 1, 8-10) design process.

Claim 28. The method defined in claim 25, wherein the design flow is associated with a programmable logic design process (column 1, 8-10).

Claim 32. The method defined in claim 1, additionally comprising performing a logical transformation on the first node if the reducing delays (column 4, lines 40-54) for at least one of the set of fanins (column 15, lines 22-25) with negative slack (positive and negative slack: column 10, lines 40-54) values of the first node is not successful.

Claim 33. The method defined in claim 25, wherein reducing delays (column 4, lines 40-54) associated with the fanins (column 15, lines 22-25) of the first node is performed before any local transformation of the first node.

Claim 34. The method defined in claim 1, wherein sorting fanins (column 15, lines 22-25) of the first node includes sorting fanins (column 15, lines 22-25) of the first node in order according to slack (positive and negative slack: column 10, lines 40-54) values associated with the corresponding fanins (column 15, lines 22-25).

Claim 35. The method defined in claim 1, wherein reducing delays (column 4, lines 40-54) associated with the fanins (column 15, lines 22-25) of the first node comprises: a) computing a delay target for each of the fanins (column 15, lines 22-25); b) determining if an arrival time for a one of the fanins (column 15, lines 22-25) is greater than the delay target for the one fanin; c) performing a delay reduction on the one fanin recursively if the arrival time for the one fanin is greater than the delay target for the one fanin; and d) repeating b) and c) for a nest fanin of the first node.

Claim 36. The method defined in claim 35, wherein reducing delays (column 4, lines 40-54) associated with fanins (column 15, lines 22-25) of the first node further comprises stopping after c) if the delay reduction of one of the fanins (column 15, lines 22-24 with column 15, lines 22-25) is not successful.

Claim 37. The method defined in claim 35, wherein the delay target for a particular fanin is based on a delay target of the first node, a pin-to-pin delay (column 15, lines 22-24; and column 30, lines 38-46) of the particular fanin, and an interconnect delay from the particular fanin (column 15, lines 22-25).

Citation of Relevant Prior Art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Chen et al., Combining Technology Mapping and Placement for Delay-Optimization in FPGA Designs" 1993 Unvi. of Tsing Hua IEEE pg.123-127.
- Cong et al., "Delay-Optimal Technology Mapping for FPGAs with Heterogeneous LUTs" 1998 ACM pg.704-707.
- Murgai et al., "Performance Directed Synthesis for Table Look Up Programmable Gate Arrays" 1991 IEEE pg.572-575.
- Changfan et al., "Timing Optimization on Routed Design with Incremental Placement and Routing Characterization" 2000 IEEE pg.188-196.

Section II: Response to Applicants' Arguments

6. Applicant's arguments with respect to the rejection to all claims of the last office action have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Bennett et al.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Leo Picard ((571) 272-3749). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Should the applicant(s) have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

October 24, 2005

TS

Paul L. Rodriguez 10/28/05
Primary Examiner
Art Unit 2125